Hall Ticket Number:

Code No, : 22605

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.E. (ECE: CBCS) II-Semester Main Examinations, July-2017

(Embedded Systems & VLSI Design)

VLSI Physical Design

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. List the various layers of VLSI.
2. Why inductor is difficult to fabricate in IC's?
3. Distinguish between stick diagrams and layouts.
4. Mention the purpose of **vias** in layouts.
5. Write any two scalable CMOS design rules.
6. Draw the layout of CMOS inverter.
7. "Is cell based design useful for analog integrated circuits", Justify.
8. What is the effect of FET orientation on cell dimensions?
9. Write the significance of LVS in designing IC's.
10. Are there any advantages of using CAD tools, list all of them.

Part-B (5 × 10 = 50 Marks)

11. a) What are the various steps in NMOS fabrication process? [5]
    b) Briefly explain lateral and vertical structure of BJT. [5]
12. a) What is latch up problem? [3]
    b) Explain about device matching and common centroid techniques for analog circuits. [7]
13. a) Draw the circuit and Layout of three inputs NOR gate. [5]
    b) For the given expression $f = \overline{p(q+r)+sv}$; draw the stick diagram. [5]
14. a) There are many issues in large scale physical design, explain in brief. [5]
    b) Explain about Wein berger image array technique and write its merits and demerits. [5]
15. a) Explain Pre and Post level simulation in designing IC. [6]
    b) What are the various CAD tools used in VLSI physical design? [4]
16. a) List out the different metals used in interconnects and write their merits and demerits. [5]
    b) Explain the purpose of dummy transistors and dummy resistors. [5]
17. Write short notes on any ***two*** of the following:
    a) Hierarchical stick diagram [5]
    b) H-tree clock distribution [5]
    c) Silicon compiler. [5]